Review of Majority Logic-Based Approximate Adders and Multipliers for Emerging Nanotechnologies

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Abstract: *The increasing demand for high-performance and energy-efficient computing has driven significant interest in approximate computing, particularly for error-tolerant applications such as image processing, multimedia, and machine learning. Majority Logic (ML) has emerged as a promising paradigm for implementing approximate arithmetic circuits in emerging nanotechnologies like Quantum-Dot Cellular Automata (QCA), nanomagnet logic, and spin-wave devices, owing to its compact design, low power consumption, and scalability. This review presents a comprehensive study of ML-based approximate adders and multipliers, focusing on their architectural classifications, key design principles, and performance trade-offs. Various state-of-the-art designs, including MLAFA-a, MLAFA-b, and ML-based approximate compressors, are analyzed in terms of logic complexity, delay, power efficiency, and accuracy metrics such as Mean Absolute Error (MAE) and Normalized Mean Error Distance (NMED). Special emphasis is placed on their applicability in error-resilient domains, where near-perfect output quality can be maintained despite intentional inexactness. The review also highlights current challenges, emerging trends, and future research opportunities, aiming to guide further advancements in ML-based approximate arithmetic for nanoscale systems.*

Keywords: *Majority Logic, Approximate Computing, Quantum-Dot Cellular Automata, Approximate Adders, Approximate Multipliers, Nanotechnology*

I. INTRODUCTION

The rapid growth of error-tolerant computing applications such as image and video processing, multimedia systems, and machine learning has shifted design priorities from absolute accuracy to a balance between performance, power efficiency, and acceptable output quality[1]. In these domains, minor computational inaccuracies have negligible perceptual impact, allowing designers to trade precision for significant improvements in speed and energy efficiency. However, conventional CMOS technology is approaching its physical and scaling limits, facing challenges such as increased leakage currents, high power density, and reduced device reliability at nanometer scales. These limitations have accelerated the exploration of new paradigms like approximate computing, where controlled inaccuracies can yield substantial benefits in performance and resource utilization[2].
Majority Logic (ML) operates on the principle that a gate's output reflects the majority value among its inputs, typically three or more. This abstraction allows complex Boolean functions to be realized with fewer gates compared to traditional logic. Unlike conventional Boolean designs that rely heavily on AND, OR, and XOR, ML's generalized approach simplifies certain arithmetic operations and aligns naturally with novel nanotechnologies. In particular, Quantum-Dot Cellular Automata (QCA), nanomagnet logic, and spin-wave devices leverage ML as a fundamental building block, offering advantages such as ultra-low power consumption, reduced interconnect complexity, and high functional density characteristics that make ML especially relevant for next-generation approximate computing architectures[3] .

This review focuses on ML-based approximate adders and multipliers, emphasizing their design principles, trade-offs, and performance in emerging nanotechnologies. Key evaluation parameters include accuracy metrics (MAE, NMED), power consumption, delay, and area efficiency, enabling a comprehensive comparison across existing architectures. Special attention is given to their integration in error-resilient applications, notably image processing, machine learning accelerators, and low-power embedded systems. By surveying state-of-the-art designs and analyzing their relative strengths and weaknesses, this review aims to highlight current advancements, identify persistent challenges, and suggest directions for future research in ML-based approximate arithmetic[4].

II. FUNDAMENTALS OF MAJORITY LOGIC-BASED APPROXIMATE COMPUTING

Approximate computing is a design paradigm that intentionally relaxes computational accuracy to achieve significant improvements in performance, power efficiency, and circuit complexity. The fundamental trade-off lies between error tolerance and resource optimization, where applications can tolerate slight deviations from exact results without noticeable degradation in output quality. This approach is particularly effective in domains such as image and video

processing, multimedia applications, wireless communication, and machine learning, where human perception or algorithmic resilience masks minor computational errors. By exploiting this flexibility, designers can create hardware architectures that are faster, consume less energy, and occupy less silicon area.

At the core of majority logic-based designs is the majority gate, which outputs the value held by the majority of its inputs, typically three. The majority function can be expressed as M(A,B,C)=AB+AC+BCM(A, B, C) = AB + AC + BCM(A,B,C)=AB+AC+BC, and it can be reduced to conventional AND or OR operations by fixing one input to logic '0' or '1'. While ML simplifies many logic functions, implementing XOR/XNOR in ML is more challenging, often requiring multiple majority gates and inverters, which can increase logic depth and delay. These properties influence the architectural choices in approximate arithmetic design, as XOR-based operations are common in adders and multipliers.

Several emerging nanotechnologies naturally support ML as their primary computation model. Quantum-Dot Cellular Automata (QCA) exploit electron position to represent binary states, enabling ultra-low power and high-density logic implementations. Nanomagnet logic uses magnetic orientations for computation, offering non-volatility and scalability, while spin-wave devices employ wave interference for signal processing with minimal energy dissipation. Compared to CMOS, these technologies promise reduced interconnect complexity, lower power consumption, and higher functional density, making them ideal platforms for implementing ML-based approximate arithmetic circuits in next-generation computing systems[3], [5], [6].

III. REVIEW OF ML-BASED APPROXIMATE ADDERS

ML-based approximate adders can be broadly classified based on their bit-width and carry chain dependency. Bit-width classifications include simple 1-bit designs, small-scale 2-bit and 4-bit architectures, and larger n-bit implementations for more complex operations. Another important distinction is between cascaded and non-cascaded designs: cascaded architectures link smaller adders in sequence, making them susceptible to error propagation through the carry chain, while non-cascaded designs eliminate such dependencies, significantly reducing cumulative errors and improving delay performance. This classification is critical in determining design trade-offs between hardware complexity, accuracy, and scalability.

Several notable ML-based approximate adder architectures have been proposed in the literature. The MLAFA-a and MLAFA-b designs optimize majority gate usage while controlling maximum absolute error, with MLAFA-b offering reduced logic depth by eliminating carry chain dependencies. Other architectures, such as the Most Significant Adder (MSA) and Least Significant Adder (LSA), selectively apply exact and approximate logic to specific bit segments, enabling accuracy tuning. XOR/XNOR-based designs simplify sum computation but often incur higher ML gate counts due to XOR's implementation complexity in majority logic. Reverse Carry Propagation Adders (RCPA) present another approach, reversing the carry flow to improve stability under delay variations[2], [7]–[9] .

Performance evaluations of these designs typically focus on logic complexity measured in terms of majority gates, inverters, and logic depth and on accuracy metrics such as Mean Absolute Error (MAE), Normalized Mean Error Distance (NMED), and Mean Error Distance (MED). QCA-based implementations further reveal the relationship between logical efficiency and physical cost, with well-optimized designs reducing cell count, area, and clocking phases. Comparisons show that non-cascaded designs like MLAFA-b and hybrid approaches (e.g., LSA-MSA combinations) achieve superior accuracy while maintaining compact layouts, making them promising candidates for low-power, high-performance nanotechnology applications [10], [11]

IV. REVIEW OF ML-BASED APPROXIMATE MULTIPLIERS

In majority logic (ML)-based multiplier design, compressors play a central role in partial product reduction, directly influencing performance, area, and power efficiency. The Partial Product Reduction (PPR) circuitry is particularly significant, as its structure determines both the delay of the multiplier and its susceptibility to error accumulation. Efficient PPR design can substantially lower logic depth and gate count while maintaining acceptable accuracy, making it a key optimization target in approximate multipliers for nanotechnology-based implementations .

Existing ML-based approximate multiplier architectures leverage various compressor configurations. Traditional 4:2 compressor-based designs are widely used due to their simplicity, while more advanced 6:3 compressors, such as the ML-based Approximate Parallel Compressor (MLAPC), offer higher compression rates with fewer gates. Integration with reduction schemes like Wallace tree and Dadda-based approaches enables faster multiplication by minimizing the number of reduction stages. The MLAPC, in particular, achieves significant hardware savings by discarding selected inputs and simplifying output computation, making it especially suited for low-power and high-speed applications.

Performance evaluations of these multipliers consider hardware cost metrics such as the number of majority gates, inverters, physical area, delay, and power consumption alongside accuracy indicators like Mean Absolute Error (MAE) and Normalized Mean Error Distance (NMED). Case studies in image processing show that optimized ML-based multipliers can produce near-identical outputs to exact designs, achieving high SSIM and PSNR values, while neural network accelerators built on these multipliers sustain competitive classification accuracy with reduced energy budgets. These results demonstrate that ML-based approximate multipliers, when carefully designed, can deliver substantial performance and efficiency benefits for error-tolerant applications [12]–[15].

V. CHALLENGES, TRENDS, AND FUTURE DIRECTIONS

Despite significant progress, ML-based approximate designs face notable limitations. Carry propagation errors remain a primary concern, especially in larger bit-width adders and multipliers where inaccuracies can accumulate and degrade output quality. The realization of XOR gates in ML logic is inherently complex, often requiring multiple stages and increasing logic depth, which impacts delay and area efficiency. Furthermore, scalability challenges arise when extending designs to higher bit-widths, as maintaining low error rates while controlling hardware cost becomes increasingly difficult.

Recent research trends aim to address these issues through hybrid exact-approximate architectures that selectively apply approximation to error-tolerant sections of a circuit, balancing accuracy and efficiency. Reconfigurable accuracy designs are gaining attention, enabling dynamic trade-offs between precision and performance based on application needs. Additionally, AI-assisted design space exploration is emerging as a powerful tool for optimizing ML-based circuits across multiple metrics. Looking ahead, opportunities exist in integrating ML-based approximate designs into neuromorphic computing for brain-inspired architectures, leveraging advances in QCA and spin-wave fabrication to enhance performance and manufacturability, and developing cross-technology portable designs that can be efficiently implemented across diverse nanoscale platforms [16]–[19].

VI. CONCLUSION

Majority Logic-based approximate adders and multipliers represent a compelling direction for achieving high efficiency in error-tolerant computing, especially when implemented in emerging nanotechnologies. Their ability to balance power, area, and performance with acceptable accuracy makes them ideal for next-generation applications in image processing, neural network acceleration, and low-power embedded systems. While challenges such as carry error propagation, XOR implementation complexity, and scalability persist, advancements in hybrid architectures, reconfigurable accuracy designs, and fabrication technologies are paving the way for more robust and efficient solutions. Continued research and cross-disciplinary innovation will be key to fully unlocking the potential of ML-based approximate arithmetic in future computing paradigms.

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